Department of Computer Science
Duke University
Ph.D. Qualifying Exam

Computer Architecture

Instructions

- Answer all 6 (SIX) of the questions.
- Write your code number on each page of this exam.
- State all of your assumptions explicitly.
- Show all of your work.
- You have three (3) hours to complete this exam.

- This is a closed book exam.
- Calculators are permitted, but are not required to complete the exam.

Policy on Misprints and Ambiguities

We have made every effort to carefully proofread this exam, and make the questions clear and concise. If you believe a problem is stated incorrectly, notify the proctor immediately. In any event, include your interpretation of the problem in your written answer.

Good Luck!

Question 1: What is Amdahl's Law? Write down the equation and then explain in words why computer architects care about it. If you don't remember the equation, please explain its qualitative meaning.

Question 2: Define what it means for a processor to have “precise interrupts” and then explain how a dynamically scheduled processor core can use a reorder buffer (ROB) to support precise interrupts.

Question 3: You are deciding between Cache Hierarchy CA and Cache Hierarchy CB. Your only criterion is performance. Which do you choose and why? Show your math.

	CA	**CB**
L1D size	64KB	64KB
L1D associativity	1-way	2-way
L1 access latency (hit or miss)	1 cycle	2 cycles
L1 miss rate	10%	5%
L2 size	2MB	1MB
L2 access latency	15 cycles	10 cycles
L2 miss rate	5%	10%
main memory	200 cycles	200 cycles

Question 4: Assume a 64-bit machine with a 2-way set-associative 4KB virtual cache that has 16-byte blocks. Assume the following sequence of load addresses. Assume LRU replacement and assume all frames are initially invalid.

address	hit or miss?	set index (base 10)?	block offset (base 10)?
7			
17			
31			
0			
2049			
15			
4099			
2048			
3			
20			

Question 5: Assume a 32-bit machine with a 32KB page size. Assume 2GB of physical memory. Write your answers in the form of 2^X rather than trying to figure out what that corresponds to. E.g., don't write out 2048 - write 2^{11} instead.

(a) How many virtual pages are there per process?

(b) How many bits are needed to represent the virtual page number?

(c) How many bits are needed to represent the virtual page offset?

(d) How many bits are needed to represent the physical page offset?

(e) How many page table entries are there per process if we use a flat page table?

Question 6: (a) Many multicore processors provide cache coherent shared memory. Explain how, in a multicore **without** a cache coherence protocol, a cache could end up with incoherent data.

(b) Define sequential consistency.