Department of Computer Science
Duke University
Ph.D. Qualifying Exam

Computer Architecture

Instructions

- Answer all questions: some questions may have several parts.

- **Write your code number on each page of this exam**.

- Be sure to provide code sequences and/or examples to support answers when requested.

- State all of your assumptions explicitly.

- Show all of your work.

- You have three (3) hours to complete this exam.

- This is a closed book/notes exam.

Policy on Misprints and Ambiguities

We have made every effort to carefully proofread this exam, and make the questions clear and concise. If you believe a problem is stated incorrectly, notify the proctor immediately. In any event, include your interpretation of the problem in your written answer.

Good Luck!

Question 1. Performance

a) [10 pts] Processor P has a 1ns clock cycle time with CPIs of: LD 3, ST 1, FADD 1, FMUL 3, FDIV 12. Given a program that executes 10 Million instructions with the instruction compositon of LD 30%, ST 20%, FADD 25%, FMUL 15%, FDIV 10%, compute the execution time on processor P. Show your work.

b) [10 pts] An optimization reduces the time for function A by a factor of 20. Compute the speedup achieved by this optimization for two programs P1 and P2 for the following two cases: A is 20% of P1 and it is 60% of P2. Show your work.

Question 2. Pipelining

a) [10 pts] Explain how pipelining can improve performance of a processor. Provide an assembly code sequence as an example to support your explanation. Comment your code as needed.

b) [5 pts] What is a structural hazard in a pipeline? In one sentence, explain how structural hazards limit performance.

c) [5 pts] What is a branch target buffer and how does it help improve pipelined processor performance?

Question 3. Processor Design

a) [15 pts] Explain why register renaming is important and describe one way to implement renaming. Use a short code sequence to demonstrate your implementation and show how it improves performance compared to a processor without register renamining.

b) [5 pts] Write a short assembly code sequence that exhibits high amounts of instruction level parallelism for a statically scheduled two-issue superscalar processor.

Question 4. Memory Hierarchies

a) [5 pts] Write down the average memory access time equation for a two level cache hiearchy.

b) [15 pts] Assume a system has 64-bit virtual addresses, 40-bit physical addresses, and 8 KB virtual memory pages. Draw a block diagram of the following memory system. A 256 entry direct-mapped TLB, a 128 KB 2-way set-associative physically indexed, physically tagged, write-back cache, with 128 Byte blocks. Draw a block diagram of this memory hierarchy. Clearly indicate how many bits are used for the index and tag of each structure, and how the appropriate data is selected assuming full word (64-bit) load/store instructions. Also clearly show where the TLB is placed with respect to the cache.

Question 5. Miscellaneous Topics

a) [5 pts] Briefly explain the difference between software pipeline and loop unrolling.

b) [8 pts] Can a cache coherent multiprocessor with a write buffer provide sequential consistency? Explain your answer using an example code sequence.

c) [7 pts] Explain how Simultaneous Multi-Threading (SMT) used in general purpose processors differs from Single Instruction Multi-Threading (SIMT) used in GPUs.