DUKE
COMPUTER SCIENCE

Efficient Algorithms for Design Automation of Flow-Based Microfluidic Biochips

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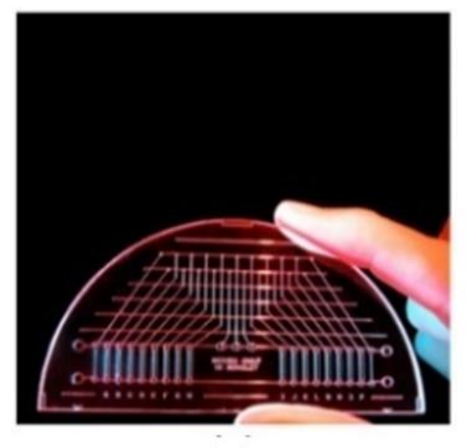
Research

Abstract

- Microfluidics emerged as on-chip solution for executing bioassays - biomolecular research.
- Flow-based microfluidics: emerging technology to handle scalable biological operations
- Chip-to-world interfacing requires reducing on-chip area overhead caused by pins and world off-chip area caused by external sources
- Growing need for to improve chip performance and optimize resources for enhanced architectural-level design



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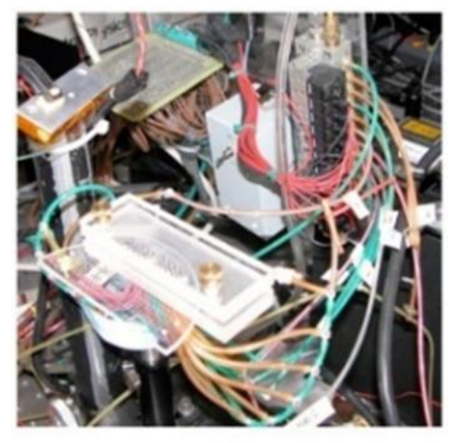

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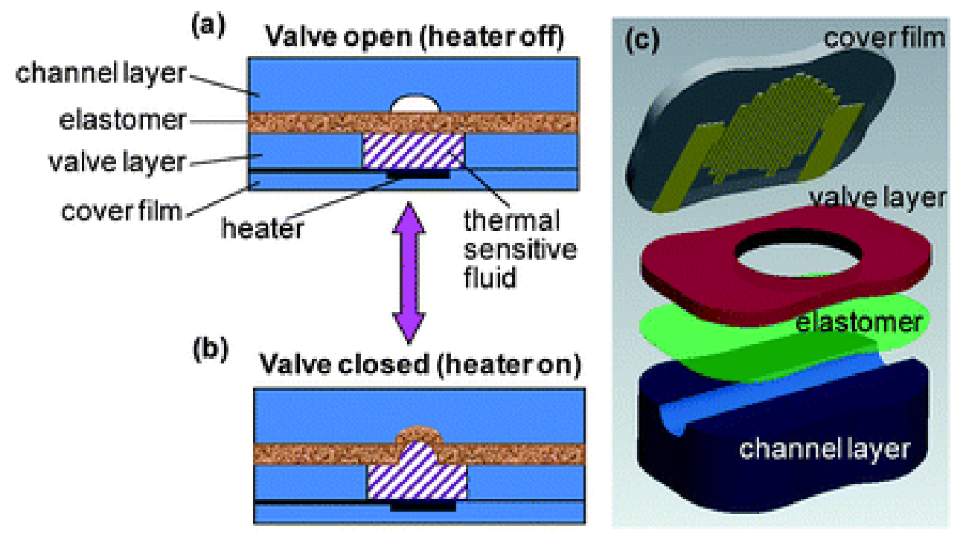


Chip-to-World Interfacing

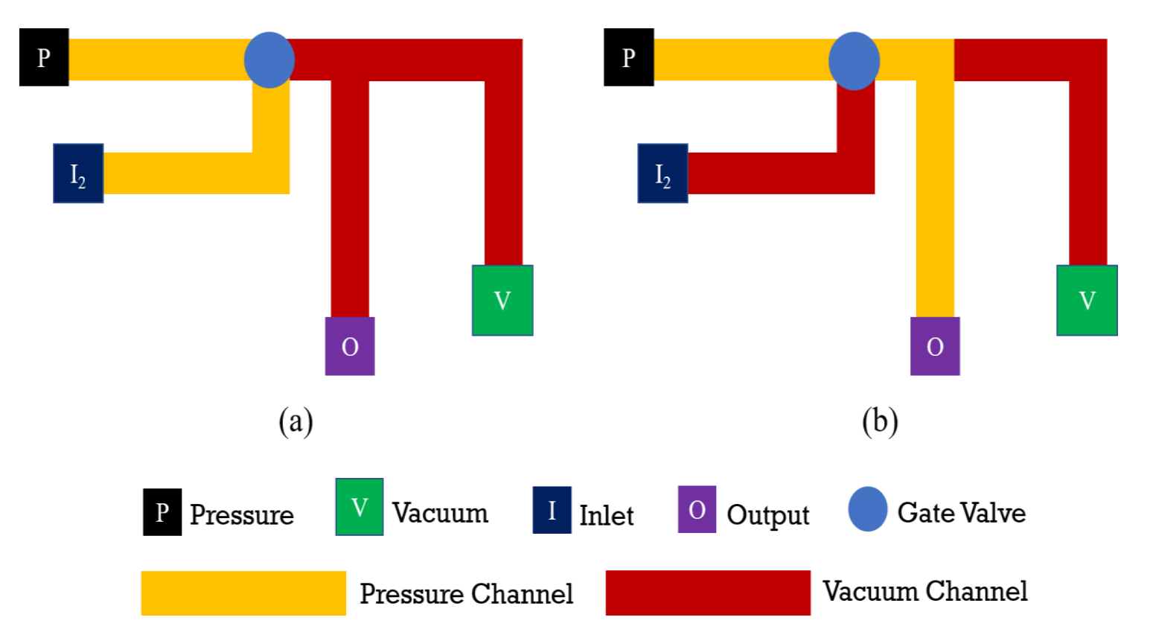
- **Goal:** Address scalable valve control for design automation and synthesis in flow-based microfluidics
- **Approach:** Create a fluidic interface among biochip components, i.e., valves, channels, and external pumps, to scale real world with microfluidic devices – "chip-to-world interfacing"
  - ✓ Reduce expensive, bulky, and power-hungry off-chip control via control-pin minimization
  - ✓ Control-pin minimization using linear algebra (Gauss-Jordan elimination) and logic gates
  - ✓ Pins actuate/control microfluidic valves, which drive fluid through a network
  - ✓ Valve states are "open" (1), "closed" (0), or "don't care" (X)
  - ✓ Actuation sequence = Sequence of states for a valve over all time steps
  - ✓ Map electrical circuits constructed using logic gates to microfluidic/pneumatic circuits
- Direct-pin addressing poses a challenge
- Look at table of actuation sequences to pinpoint patterns for pin-count minimization

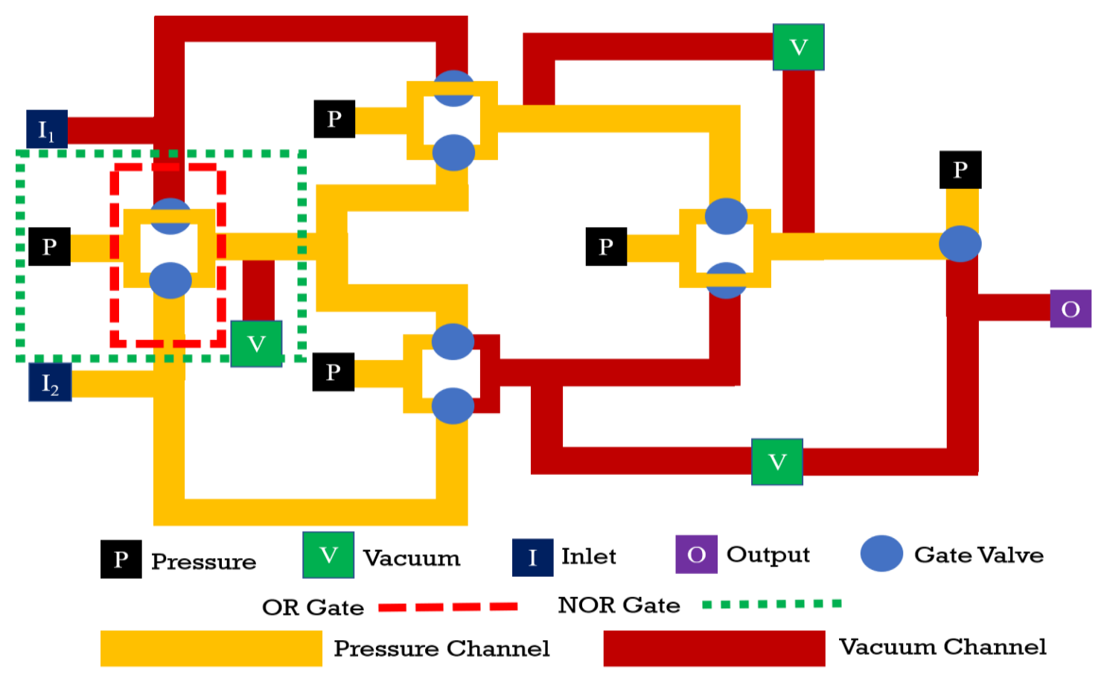
Step	V_1	V_2	V_3	V_4	V_5	V_6	V_7	V_8	V_9	V_{10}
1	0	1	1	0	0	1	0	0	1	0
2	0	0	1	1	1	0	1	1	0	1
3	1	1	0	0	1	0	1	1	0	1
4	X	1	X	0	1	0	X	X	0	1
5	X	0	X	1	0	1	X	0	0	1

Microfluidic Logic Gates

- Just as electrical logic gates are used in today's integrated circuits, microfluidic logic gates can be used to implement basic Boolean operations (e.g. *AND*, *OR*, and *NOT*)
- We use XOR and NOT microfluidic gates
- Advantages of microfluidic gates
  - ✓ Use limited number of control pins
  - ✓ Offer large space of microfluidic capabilities leveraged for pin-constrained designs
  - ✓ **Microfluidic complexity**: The number of valves, $9j + k$, used to represent j *XOR* gates and k *NOT* gates (analogy to electrical circuit complexity)

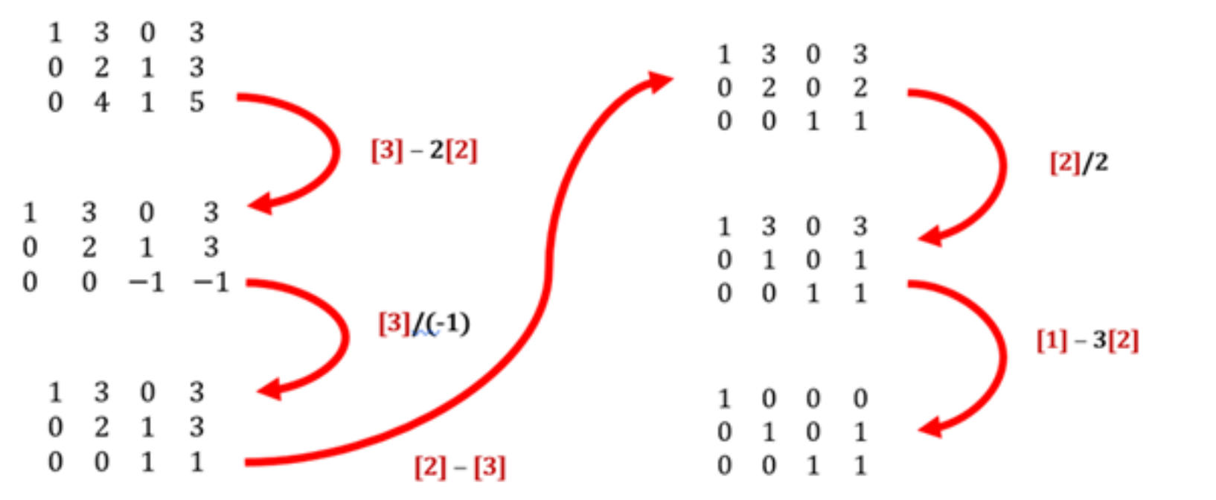
Electrical Component	Microfluidic Component
Power	Vacuum Source
Ground	Atmospheric Pressure
Closed Switch	Open Valve
Open Switch	Closed Valve





Modeling Using Linear Algebra

- Previous work modeled pin-constrained design using techniques from graph theory
- We use linear algebraic modeling due to the use of on-chip microfluidic gates and Boolean logic operations
- We reduce the number of control pins using linear operations defined by a linear algebraic mapping function
- **Question:** can we represent an actuation sequence vector as a linear combination of other actuation sequence vectors?
- Linear Algebra
  - ✓ An "automatic" solution to the above question
  - ✓ Gauss-Jordan Elimination: Linear algebraic technique used to find a basis of elements from a vector space in order to solve a linear system of equations
  - ✓ XOR-based modification uses XOR operations in place of the elementary row operations
  - ✓ Method referred to as "XGJE"



Problem Formulation

- **Input**: The set of actuation vectors
- **Objective**: Minimize the number of control pins used to actuate n valves
- **Constraints**: User constraints on the number of pins and the number of additional valves for microfluidic gates
- **Output**: The minimized pin-count; the set of pin actuations

Solution

- **Compatibility Analysis**: Address nonlinearity of NOT gates and existence of don't-care states by a process called "Don't-Cares and Complements Struct Traversal" (DCSST)
- **Pin-Count Minimization Technique**: Perform XGJE after DCSST to obtain a set of pin actuations
- **Microfluidic Circuit Design**: Construct microfluidic circuit to represent actuations in pin-constrained design by a process called "Node-Traversal Circuit Optimization (NTCO)" and perform tradeoff analysis of pin-count vs. microfluidic complexity

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Algorithm 1 Synterface
Input: Set of actuation vectors $\Gamma$, maximum constraint on pins $P_{max}$ and on valves $V_{max}$
Output: $S$, the list of solution sets $\{q, \eta, MC\}$
$\{MC, i, S\} \leftarrow 0$
findComplementsAndDontCares($\Gamma$)
$\Omega \leftarrow$ XORGaussJordanElimination($\Gamma$)
$\{q, \eta\} \leftarrow$ determineActuationPins($\Omega, \Gamma$)
while $q < P_{max}$ and $MC < V_{max}$ do
    $\{q_{new}, \eta_{new}, MC\} \leftarrow$ NTCO($q, \eta, \Gamma$)
    $S[i] \leftarrow$ storeSolution($q_{new}, \eta_{new}, MC$)
    $i \leftarrow i + 1$; $q \leftarrow q_{new}$; $\eta \leftarrow \eta_{new}$
return $S$
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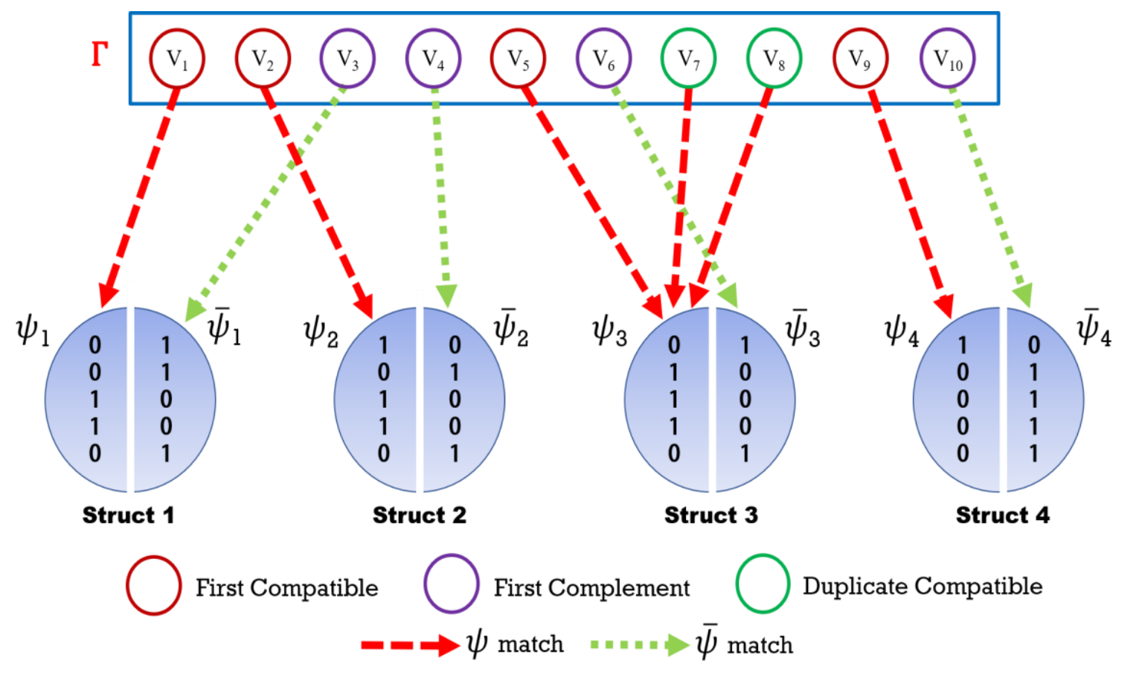
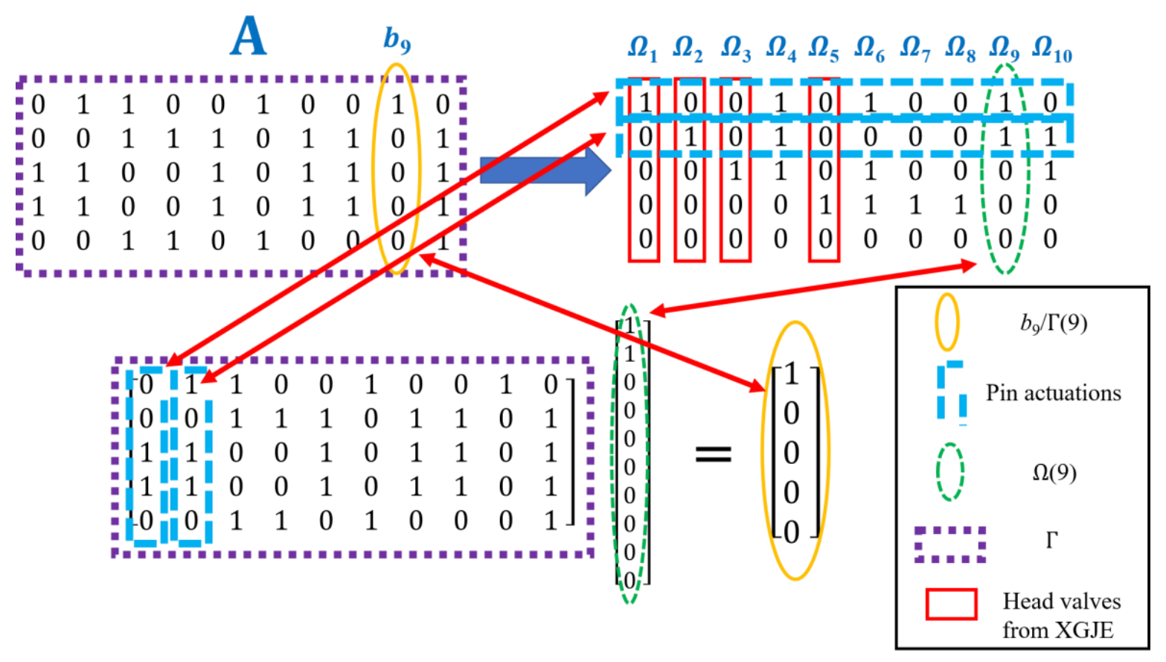




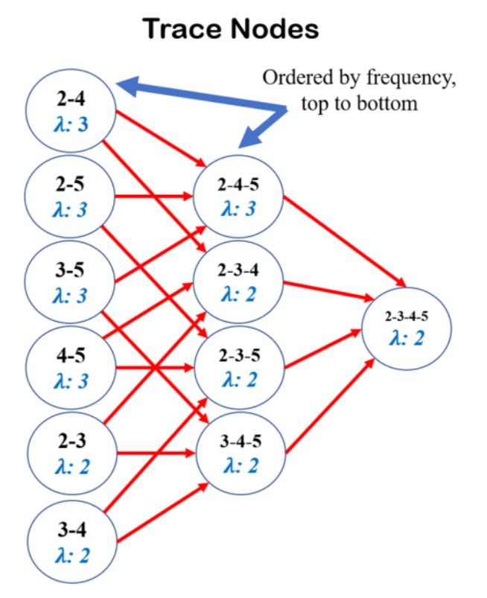
Actuation Sequences

1: 1
4: 4
7: 2-3-4-5
2: 2
5: 5
8: 2-4-5
3: 3
6: 1-2-3-4-5
9: 3-5

Sequence Nodes

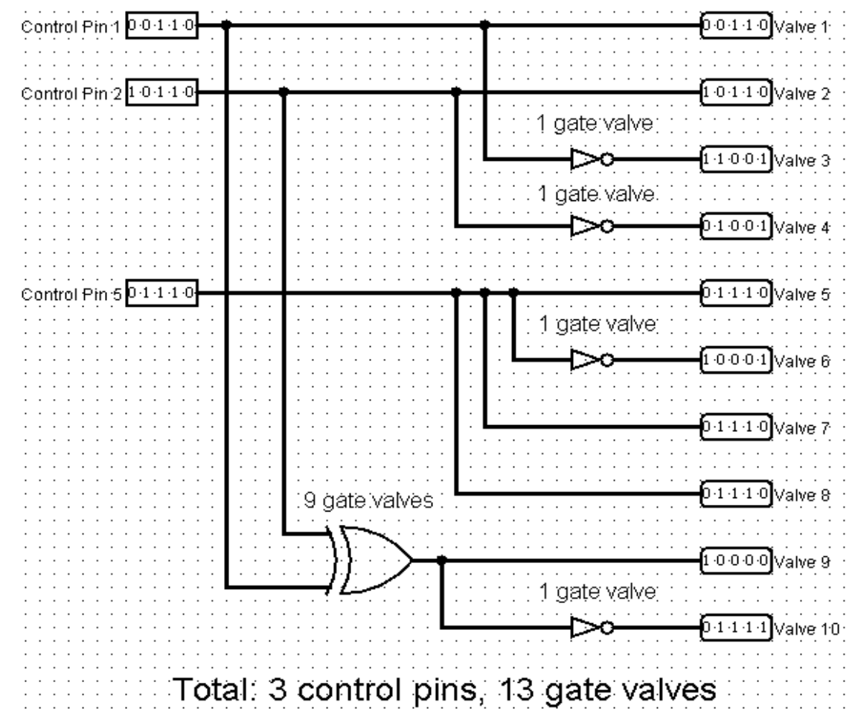
	Sequence Nodes	Trace Nodes	Constructed	Leftover
Step 1	***6***: 1-2-3-4-5 ***7***: 2-3-4-5 ***8***: 2-4-5 ***9***: 3-5	2-4 2-4-5 2-3-4-5	***6***: 2-3-4-5 ***7***: 2-3-4-5 ***8***: 2-4-5 ***9***:	***6***: 1 ***7***: ***8***: ***9***: 3-5
Step 2	***6***: 1-2-3-4-5 ***7***: 2-3-4-5 ***8***: 2-4-5 ***9***: 3-5	2-5 2-3-5	***6***: 2-3-4-5 ***7***: 2-3-4-5 ***8***: 2-4-5 ***9***:	***6***: 1 ***7***: ***8***: ***9***: 3-5
Step 3	***6***: 1-2-3-4-5 ***7***: 2-3-4-5 ***8***: 2-4-5 ***9***: 3-5	3-5 3-4-5	***6***: 2-3-4-5 ***7***: 2-3-4-5 ***8***: 2-4-5 ***9***: 3-5	***6***: 1 (+1 XOR) ***7***: ***8***: ***9***:

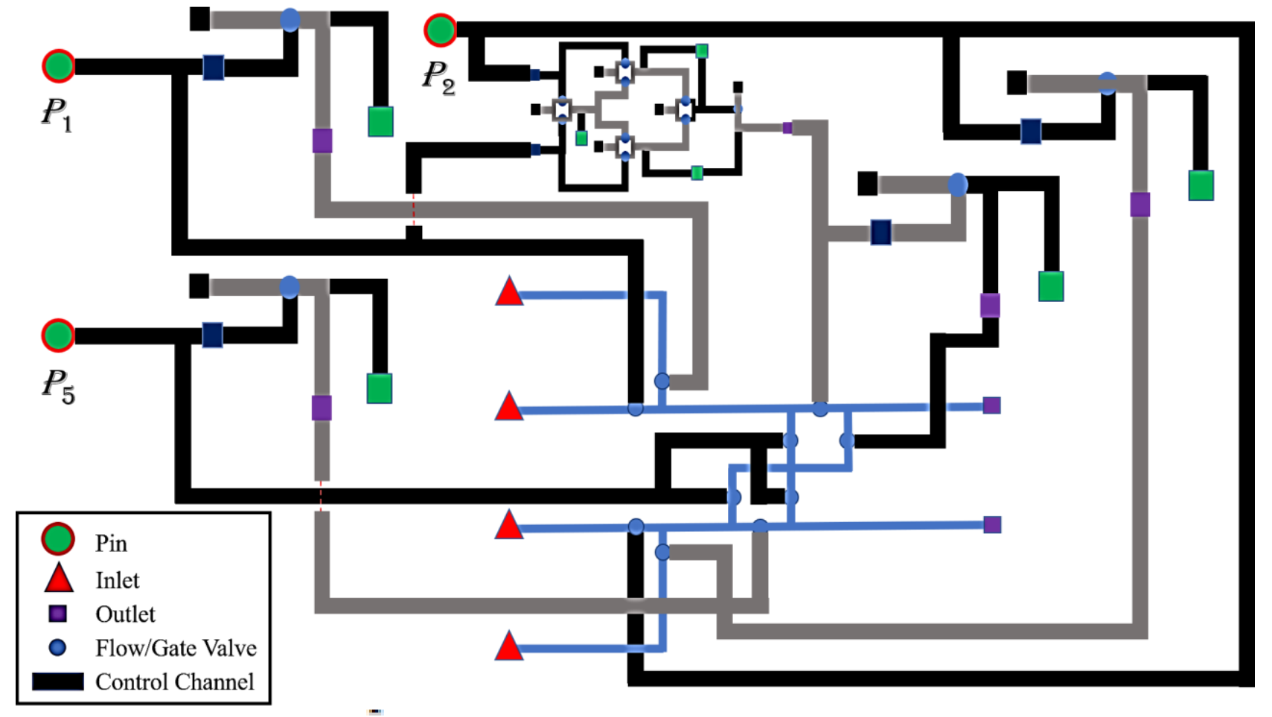
Trace Nodes



Experimental Results

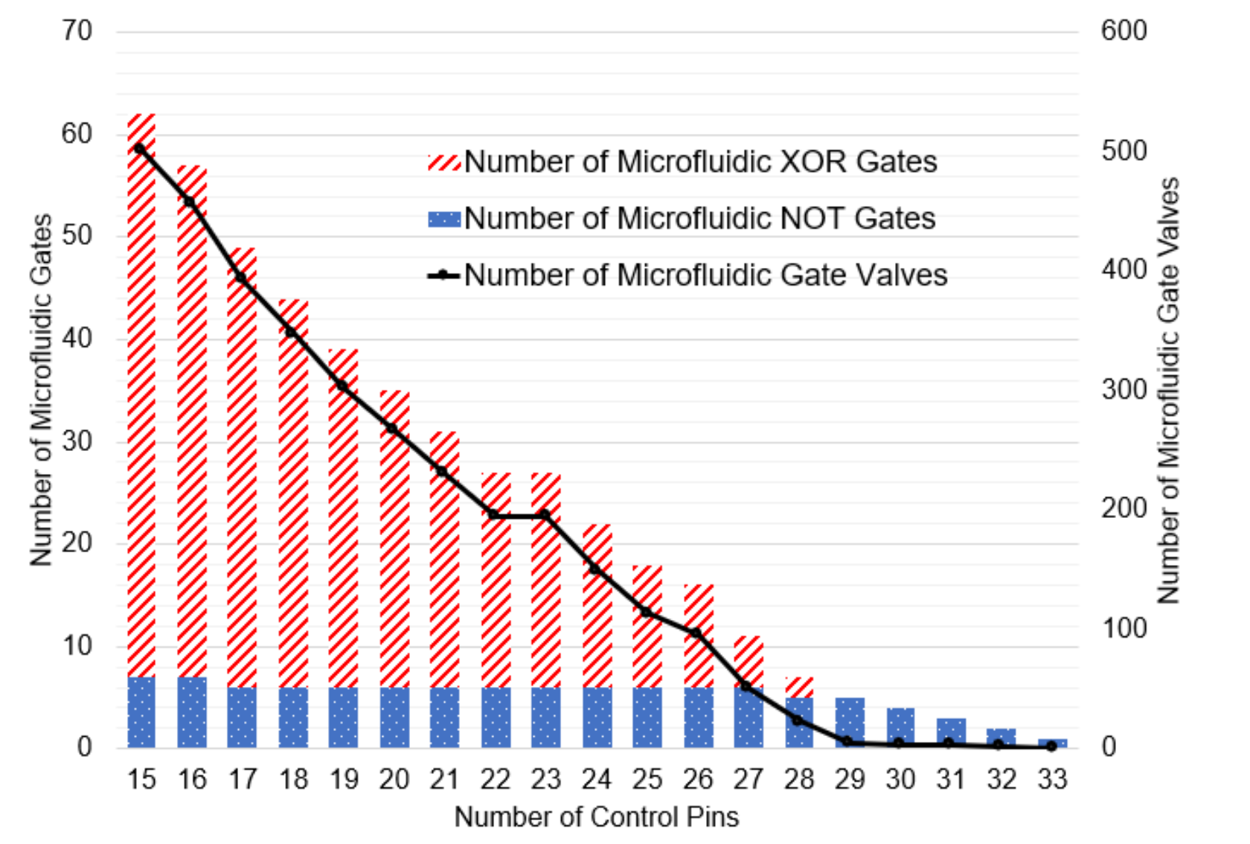
- Performance evaluated using two primary metrics: (1) the number of control pins, and (2) the microfluidic complexity
- We compare NTCO to a brute-force algorithm that computes all permutations of logic circuit arrangements and chooses arrangement with least microfluidic complexity





Microfluidic Application	Number of Valves	Number of Time Steps	Number of Control Pins		Number of Gate Valves
			Valve Sharing [19]	Our Solution	
4-to-2 Crossbar Application	10	5	8	3	13
Rotary Mixer	14	96	10	7	37
8-to-4 Crossbar Application 1	80	6	4	2	2
8-to-4 Crossbar Application 2	80	17	36	15	502
ChIP	56	33	14	11	74
HTChIP	176	14	15	11	91

Microfluidic Application	Brute-Force Runtime (s)	NTCO Runtime (s)	Pin Overhead (mm^2)		Valve Overhead (μm^2)		Chip + World Overhead (mm^2)	
			A_{orig}	A_{opt}	A_{orig}	A_{opt}	A_{orig}	A_{opt}
4-to-2 Crossbar Application	0.0088	0.0591	20	6	360	828	48	24
Rotary Mixer	0.0754	0.0523	28	14	504	1836	58	34
8-to-4 Crossbar Application 1	0.0072	0.0505	160	4	2880	2952	336	28
8-to-4 Crossbar Application 2	N/A	0.1299	160	30	2880	20952	336	80
ChIP	N/A	0.0691	112	22	2016	4680	240	64
HTChIP	N/A	0.0670	352	22	6336	9612	756	100



Conclusions

- Presented a pin-minimization solution for chip-to-world interfacing in flow-based microfluidics
- Proposed method relies uses microfluidic logic gates for on-chip valve control
- Presented a design optimization technique that uses a variant of the Gauss-Jordan elimination method from linear algebra to minimize the number of control pins
- Results show that significant reduction in the number of control pins can be achieved with very little impact on chip area in terms of additional valves needed for the microfluidic logic gates
- Future work: integrate Quine-McCluskey algorithm for don't-care states; implement *AND*/*OR* Boolean logic

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